What is claimed is:

1. A voltage booster for receiving a first voltage at an input and providing a boosted voltage at an output, the voltage booster comprising:

a first capacitor having a first terminal for receiving a first clock signal and having a second terminal;

a second capacitor having a first terminal for receiving a second clock signal and having a second terminal, wherein the second clock signal is complementary to the first clock signal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to receive the first voltage;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the first nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the first source/drain region of the first nFET, and the second source/drain region is coupled to the gate of the first nFET; and

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gate of the first nFET and the second source/drain region of the second nFET, the first source/drain region is coupled to the gates of the first and third nFETs and the second source/drain region of the second nFET, and the second source/drain region is coupled to the output of the voltage booster.

2. The voltage booster of claim 1, further comprising:

a fourth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to receive a control signal; and

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the third nFET and the second source/drain region is coupled to receive the control signal.

3. The voltage booster of claim 2, wherein the first and second clock signals are derived from a single clock signal.

4. The voltage booster of claim 3, wherein the control signal and the single clock signal are provided to a logic gate for selectively activating and deactivating the voltage booster.

5. The voltage booster of claim 4, wherein the logic gate is a NAND gate.

6. A pass circuit, comprising:

a first input for receiving a clock signal;

a second input for receiving a control signal;

a third input for receiving an input voltage;

an output for providing a boosted voltage;

a logic circuit having a first input coupled to the first input of the pass circuit and a second input coupled to the second input of the pass circuit, wherein the logic circuit is adapted to provide complementary clock signals in response to the control signal having a first logic value and to be deactivated in response to the control signal having a second logic value;

a first capacitor having a first terminal coupled to receive a first of the complementary clock signals and having a second terminal;

a second capacitor having a first terminal coupled to receive a second of the complementary clock signals and having a second terminal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second

terminal of the first capacitor and the first source/drain region is coupled to receive the first voltage;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the first nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the first source/drain region of the first nFET, and the second source/drain region is coupled to the gate of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gate of the first nFET and the second source/drain region of the second nFET, the first source/drain region is coupled to the gates of the first and third nFETs and the second source/drain region of the second nFET, and the second source/drain region is coupled to the output of the pass circuit;

a fourth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to the second input of the pass circuit; and

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the third nFET and the second source/drain region is coupled to the second input of the pass circuit.

7. The pass circuit of claim 6, wherein the first capacitor is sized to provide a boosted voltage at the gate of the third nFET at least equal to a value of the input voltage plus a threshold voltage of the third nFET.

8. The pass circuit of claim 6, wherein the first capacitor is sized to have a capacitance such that an amplitude of the first clock signal times a first constant is greater than a threshold voltage of the third nFET, wherein the first constant is equal to:

$$C_1 / (C_1 + C_2 + C_3 + C_4)$$

where C_1 = a capacitance of the first capacitor;

C_2 = a gate capacitance of the first nFET;

C_3 = a gate capacitance of the third nFET; and

C_4 = a capacitance at the output of the pass circuit.

9. The pass circuit of claim 8, wherein the first capacitor is sized to have a capacitance such that the amplitude of the first clock signal times the first constant is greater than the threshold voltage of the third nFET plus a threshold voltage of a pass gate coupled to the output of the pass circuit.

10. A voltage booster for receiving a first voltage at an input and providing a boosted voltage at an output, the voltage booster comprising:

a first capacitor having a first terminal for receiving a first clock signal and having a second terminal;

a second capacitor having a first terminal for receiving a second clock signal and having a second terminal, wherein the second clock signal is complementary to the first clock signal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to receive the first voltage;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the second source/drain region of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, and the first source/drain region is coupled to the first source/drain region of the first nFET;

a fourth FET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the

second nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the second source/drain region of the third nFET, and the second source/drain region is coupled to the gates of the first and second nFETs; and

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gates of the first and second nFETs and the second source/drain region of the fourth nFET, the first source/drain region is coupled to the gates of the first, second and fifth nFETs and the second source/drain region of the fourth nFET, and the second source/drain region is coupled to the output of the voltage booster.

11. The voltage booster of claim 10, further comprising:

a sixth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to receive a control signal; and

a seventh nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the fifth nFET and the second source/drain region is coupled to receive the control signal.

12. The voltage booster of claim 11, wherein the first and second clock signals are derived from a single clock signal.

13. The voltage booster of claim 12, wherein the control signal and the single clock signal are provided to a logic gate for selectively activating and deactivating the voltage booster.

14. The voltage booster of claim 13, wherein the logic gate is a NAND gate.

15. A pass circuit, comprising:

a first input for receiving a clock signal;

a second input for receiving a control signal;

a third input for receiving an input voltage;

an output for providing a boosted voltage;

a logic gate having a first input coupled to the first input of the pass circuit, a second input coupled to the second input of the pass circuit, and an output;

a first inverter having an input coupled to the output of the logic gate and an output;

a first capacitor having a first terminal coupled to the output of the logic gate and having a second terminal;

a second capacitor having a first terminal coupled to the output of the first inverter and having a second terminal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the third input of the pass circuit;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the second source/drain region of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, and the first source/drain region is coupled to the first source/drain region of the first nFET;

a fourth FET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the second source/drain region of the third nFET, and the second source/drain region is coupled to the gates of the first and second nFETs;

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gates of the first and second nFETs and the second source/drain region of the fourth nFET, the first source/drain region is coupled to the gates of the first, second and fifth nFETs and the second source/drain region of the fourth nFET, and the second source/drain region is coupled to the output of the pass circuit;

a sixth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to receive a control signal; and

a seventh nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the fifth nFET and the second source/drain region is coupled to receive the control signal.

16. The pass circuit of claim 15, further comprising:

a second inverter and a third inverter coupled in series and interposed between the second input of the pass circuit and the second input of the logic gate, wherein the second and third inverters are further interposed between the second input of the pass circuit and the second source/drain regions of the sixth and seventh nFETs.

17. The pass circuit of claim 16, further comprising:

a fourth inverter and a fifth inverter coupled in series and interposed between the output of the logic gate and the input of the first inverter, wherein the fourth and fifth inverters are further interposed between the output of the logic gate and the first terminal of the first capacitor.

18. The pass circuit of claim 15,wherein the logic gate is a NAND gate.

19. The pass circuit of claim 15, wherein the first capacitor is sized to provide a boosted voltage at the gate of the third nFET at least equal to a value of the input voltage plus a threshold voltage of the third nFET.

20. The pass circuit of claim 15, wherein the first capacitor is sized to have a capacitance such that an amplitude of the first clock signal times a first constant is greater than a threshold voltage of the third nFET, wherein the first constant is equal to:

$C_1 / (C_1 + C_2 + C_3 + C_4 + C_5)$

where C_1 = a capacitance of the first capacitor;

C_2 = a gate capacitance of the first nFET;

C_3 = a gate capacitance of the second nFET;

C_4 = a gate capacitance of the fifth nFET; and

C_5 = a capacitance at the output of the pass circuit.

21. The pass circuit of claim 20, wherein the first capacitor is sized to have a capacitance such that the amplitude of the first clock signal times the first constant is greater than the threshold voltage of the third nFET plus a threshold voltage of a pass gate coupled to the output of the pass circuit.

22. A memory device, comprising:

an array of memory cells arranged in rows and columns, with pluralities of rows of memory cells grouped in blocks;

a row decoder providing gate potentials to rows of the array of memory cells;

pass gates coupled between the row decoder and the rows of the array of memory cells for selectively passing the gate potentials to their associated rows of the array of memory cells;

a block decoder for selecting a target block of memory cells in response to a location address, wherein the block decoder comprises a pass circuit for controlling the pass gates of each block of the array of memory cells, each pass circuit comprising:

a first capacitor having a first terminal for receiving a first clock signal and having a second terminal;

a second capacitor having a first terminal for receiving a second clock signal and having a second terminal, wherein the second clock signal is complementary to the first clock signal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to receive a programming voltage;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the second source/drain region of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, and the first source/drain region is coupled to the first source/drain region of the first nFET;

a fourth FET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the second source/drain region of the third nFET, and the second source/drain region is coupled to the gates of the first and second nFETs; and

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gates of the first and second nFETs and the second source/drain region of the fourth nFET, the first source/drain region is coupled to the gates of the first, second and fifth nFETs and the second source/drain region of the fourth nFET, and the second source/drain region is coupled to the associated pass gates.

23. The memory device of claim 22, wherein the array of memory cells comprises floating-gate memory cells arranged in a NAND flash architecture.

24. A memory device, comprising:

an array of memory cells arranged in rows and columns, with pluralities of rows of memory cells grouped in blocks;

a row decoder providing gate potentials to rows of the array of memory cells;

pass gates coupled between the row decoder and the rows of the array of memory cells for selectively passing the gate potentials to their associated rows of the array of memory cells;

a block decoder for selecting a target block of memory cells in response to a location address, wherein the block decoder comprises a pass circuit for controlling the pass gates of each block of the array of memory cells, each pass circuit comprising:

a first input for receiving a clock signal;

a second input for receiving a control signal indicative of whether the associated block is selected;

a third input for receiving a programming voltage;

an output coupled to the associated pass gates;

a logic circuit having a first input coupled to the first input of the pass circuit and a second input coupled to the second input of the pass circuit, wherein the logic circuit is adapted to provide complementary clock signals when the associated block is selected;

a first capacitor having a first terminal coupled to receive a first complementary clock signal and having a second terminal;

a second capacitor having a first terminal coupled to receive a second complementary clock signal and having a second terminal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate

is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the third input of the pass circuit;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the second source/drain region of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, and the first source/drain region is coupled to the first source/drain region of the first nFET;

a fourth FET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the second source/drain region of the third nFET, and the second source/drain region is coupled to the gates of the first and second nFETs;

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gates of the first and second nFETs and the second source/drain region of the fourth nFET, the first source/drain region is coupled to the gates of the first, second and fifth nFETs and the second source/drain region of the fourth nFET, and the second source/drain region is coupled to the output of the pass circuit;

a sixth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to receive the control signal; and

a seventh nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply

voltage, the first source/drain region is coupled to the gate of the fifth nFET and the second source/drain region is coupled to receive the control signal.

25. The memory device of claim 24, wherein the first capacitor of each pass circuit is sized to provide a boosted voltage at the gate of its fifth nFET at least equal to a value of the programming voltage plus a threshold voltage of that fifth nFET.

26. The memory device of claim 24, wherein the first capacitor of each pass circuit is sized to have a capacitance such that an amplitude of the first clock signal times a first constant is greater than a threshold voltage of the fifth nFET, wherein the first constant is equal to:

$C_1 / (C_1 + C_2 + C_3 + C_4 + C_5)$

where C_1 = a capacitance of the first capacitor;

C_2 = a gate capacitance of the first nFET;

C_3 = a gate capacitance of the second nFET;

C_4 = a gate capacitance of the fifth nFET; and

C_5 = a capacitance at the output of the pass circuit.

27. The memory device of claim 26, wherein the first capacitor of each pass circuit is sized to have a capacitance such that the amplitude of the first clock signal times the first constant is greater than the threshold voltage of the fifth nFET plus a threshold voltage of an associated pass gate coupled to the output of the pass circuit.

28. The memory device of claim 24, wherein the array of memory cells comprises non-volatile floating-gate memory cells and wherein the memory cells of each column are coupled in series strings, with a first memory cell of each string selectively coupled to a bit line.

29. A method of programming a target memory cell of a memory device, comprising:

selecting a block of memory cells containing the target memory cell, wherein each block includes a plurality of rows of memory cells and wherein each of the plurality of rows of memory cells is coupled to an n-channel field-effect transistor (nFET) pass gate;

applying a programming voltage to a source/drain region of the nFET pass gate coupled to a row of memory cells containing the target memory cell;

applying an intermediate voltage to a source/drain region of the nFET pass gates coupled to remaining rows of memory cells of the selected block; and

applying a boosted voltage to gates of each of the nFET pass gates of the selected block, wherein the boosted voltage exceeds the programming voltage by at least one threshold voltage of the nFET pass gate and wherein the boosted voltage is generated by a single source.

30. A method of programming a target memory cell of a memory device, comprising:

selecting a block of memory cells containing the target memory cell, wherein each block includes a plurality of rows of memory cells, wherein each of the plurality of rows of memory cells is coupled to a first source/drain region of an n-channel field-effect transistor (nFET) pass gate and wherein the memory cells are floating-gate memory cells coupled in a NAND flash architecture;

applying a programming voltage to a second source/drain region of the nFET pass gate coupled to a row of memory cells containing the target memory cell;

applying an intermediate voltage to a second source/drain region of the nFET pass gates coupled to remaining rows of memory cells of the selected block;

generating a boosted voltage using the programming voltage, wherein the boosted voltage exceeds the programming voltage by at least one threshold voltage of the nFET pass gates; and

applying the boosted voltage to gates of each of the nFET pass gates of the selected block.

31. The method of claim 30, wherein applying the programming voltage and generating the boosted voltage occur substantially concurrently.

32. The method of claim 30, wherein the programming voltage is approximately 20V and the intermediate voltage is approximately 10V.

33. A method of programming a memory cell of a memory device, comprising:

receiving a programming command and an address at the memory device, wherein the address is indicative of a target memory cell or memory cells of the memory device and wherein the memory cells are grouped in blocks each containing a plurality of word lines;

decoding the address to identify target blocks and a target row within each target block containing the target memory cell or memory cells;

activating a pass circuit for each target block, each pass circuit receiving a programming voltage;

generating a boosted voltage on an output of each activated pass circuit, wherein the boosted voltage has a voltage level that exceeds the programming voltage;

providing each boosted voltage to a plurality of pass gates, each pass gate coupled to a row of a target block; and

providing the programming voltage to each target row through its associated pass gate receiving the boosted voltage.

34. A pass circuit, comprising:

a first input for receiving a clock signal;

a second input for receiving a control signal;

a third input for receiving an input voltage;

an output for providing a boosted voltage;

a NAND gate having a first input coupled to the first input of the pass circuit, a second input coupled to the second input of the pass circuit, and an output;

a first inverter having an input coupled to the output of the NAND gate and an output;

a first capacitor having a first terminal coupled to the output of the NAND gate and having a second terminal;

a second capacitor having a first terminal coupled to the output of the first inverter and having a second terminal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to receive the first voltage;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the first nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the first source/drain region of the first nFET, and the second source/drain region is coupled to the gate of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gate of the first nFET and the second source/drain region of the second nFET, the first source/drain region is coupled to the gates of the first and third nFETs and the second source/drain region of the second nFET, and the second source/drain region is coupled to the output of the pass circuit;

a fourth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to the second input of the pass circuit; and

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the third nFET and the second source/drain region is coupled to the second input of the pass circuit.

35. The pass circuit of claim 34, further comprising:

a second inverter and a third inverter coupled in series and interposed between the second input of the pass circuit and the second input of the NAND gate, wherein the second and third inverters are further interposed between the second input of the pass circuit and the second source/drain regions of the fourth and fifth nFETs.

36. The pass circuit of claim 35, further comprising:

a fourth inverter and a fifth inverter coupled in series and interposed between the output of the NAND gate and the input of the first inverter, wherein the fourth and fifth inverters are further interposed between the output of the NAND gate and the first terminal of the first capacitor.

37. The pass circuit of claim 34, wherein the first capacitor is sized to have a capacitance such that an amplitude of the first clock signal times a first constant is greater than a threshold voltage of the third nFET, wherein the first constant is equal to:

$C_1 / (C_1 + C_2 + C_3 + C_4)$

where C_1 = a capacitance of the first capacitor;

C_2 = a gate capacitance of the first nFET;

C_3 = a gate capacitance of the third nFET; and

C_4 = a capacitance at the output of the pass circuit.

38. The pass circuit of claim 37, wherein the first capacitor is sized to have a capacitance such that the amplitude of the first clock signal times the first constant is greater than the threshold voltage of the third nFET plus a threshold voltage of a pass gate coupled to the output of the pass circuit.

39. A memory device, comprising:

an array of memory cells arranged in rows and columns, with pluralities of rows of memory cells grouped in blocks;

a row decoder providing gate potentials to rows of the array of memory cells;

pass gates coupled between the row decoder and the rows of the array of memory cells for selectively passing the gate potentials to their associated rows of the array of memory cells;

a block decoder for selecting a target block of memory cells in response to a location address, wherein the block decoder comprises a pass circuit for controlling the pass gates of each block of the array of memory cells, each pass circuit comprising:

a first input for receiving a clock signal;

a second input for receiving a control signal indicative of whether the associated block is selected;

a third input for receiving a programming voltage;

an output coupled to the associated pass gates;

a logic gate having a first input coupled to the first input of the pass circuit, a second input coupled to the second input of the pass circuit, and an output;

a first inverter having an input coupled to the output of the logic gate and an output;

a first capacitor having a first terminal coupled to the output of the logic gate and having a second terminal;

a second capacitor having a first terminal coupled to the output of the first inverter and having a second terminal;

a first n-channel field-effect transistor (nFET) having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the third input of the pass circuit;

a second nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second terminal of the first capacitor and the first source/drain region is coupled to the second source/drain region of the first nFET;

a third nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, and the first source/drain region is coupled to the first source/drain region of the first nFET;

a fourth FET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the second source/drain region of the second nFET and the second terminal of the second capacitor, the first source/drain region is coupled to the second source/drain region of the third nFET, and the second source/drain region is coupled to the gates of the first and second nFETs;

a fifth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to the gates of the first and second nFETs and the second source/drain region of the fourth nFET, the first source/drain region is coupled to the gates of the first, second and fifth nFETs and the second source/drain region of the fourth nFET, and the second source/drain region is coupled to the output of the pass circuit;

a sixth nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive a supply voltage, the first source/drain region is coupled to the second terminal of the second capacitor and the second source/drain region is coupled to receive the control signal; and

a seventh nFET having a gate, a first source/drain region and a second source/drain region, wherein the gate is coupled to receive the supply voltage, the first source/drain region is coupled to the gate of the fifth

nFET and the second source/drain region is coupled to receive the control signal.

40. The memory device of claim 39, wherein each pass circuit further comprises:
a second inverter and a third inverter coupled in series and interposed between the second input of the pass circuit and the second input of the logic gate, wherein the second and third inverters are further interposed between the second input of the pass circuit and the second source/drain regions of the sixth and seventh nFETs.

41. The memory device of claim 40, wherein each pass circuit further comprises:
a fourth inverter and a fifth inverter coupled in series and interposed between the output of the logic gate and the input of the first inverter, wherein the fourth and fifth inverters are further interposed between the output of the logic gate and the first terminal of the first capacitor.

42. The memory device of claim 39,wherein the logic gate of each pass circuit is a NAND gate.

43. The memory device of claim 39, wherein the first capacitor of each pass circuit is sized to have a capacitance such that an amplitude of the first clock signal times a first constant is greater than a threshold voltage of the fifth nFET, wherein the first constant is equal to:

$C_1 / (C_1 + C_2 + C_3 + C_4 + C_5)$

where C_1 = a capacitance of the first capacitor;
C_2 = a gate capacitance of the first nFET;
C_3 = a gate capacitance of the second nFET;
C_4 = a gate capacitance of the fifth nFET; and
C_5 = a capacitance at the output of the pass circuit.

44. The memory device of claim 43, wherein the first capacitor of each pass circuit is sized to have a capacitance such that the amplitude of the first clock signal times the first constant is greater than the threshold voltage of the fifth nFET plus a threshold voltage of an associated pass gate coupled to the output of the pass circuit.

45. The memory device of claim 39, wherein the array of memory cells comprises non-volatile floating-gate memory cells and wherein the memory cells of each column are coupled in series strings, with a first memory cell of each string selectively coupled to a bit line.